1 Description

- Featured part: Xilinx® CoolRunner-II® XC2C32A
  - 32-macrocell CPLD
- Modified DIP-40 footprint
  - .100" pin spacing
  - Breadboard-able
  - 17 usable I/O
- Micro-B connector for power
- External power up to 6.0V
- 1.8V and 3.3V LDO
  - VCCIO Bank 1: fixed 3.3V
  - VCCIO Bank 2: selectable 1.8V/3.3V
- On-board clock sources
  - 8.0 MHz MEMS oscillator
  - 7.8125 kHz ($1{:}2^{10}$ divider)
- On-board GSR push-button
  - De-bounce filter
- JTAG programming header

The *XCtiny* is a low-cost development platform featuring the small-scale XC2C32A CoolRunner-II® complex programmable logic device (CPLD) from Xilinx®.

The board's DIP-40 footprint with standard .100" pin spacing makes it ideal for use in prototyping on a solderless breadboard. The board can be supplied via an external power supply with up to 6.0V, or via the Micro-B connector. Two on-board LDO regulators provide the necessary supplies for the CPLD, allowing for an external supply voltage as low as 4.0V.

One of the I/O bank supply voltages is user-selectable via a jumper link, allowing the board to interface with common 3.3V, as well as low-power 1.8V peripherals.

On-board peripherals include two clock sources: the signal of an 8.0MHz MEMS oscillator is connected to one of the Global Clock inputs (GCK) of the CPLD. This clock signal is further connected to an external 10-stage clock divider, providing a low-frequency clock source of 7.8125kHz.

A push-button with dedicated debounce circuitry is connected to the Global Set/Reset input (GSR). All remaining GPIO are fanned out to breadboard pins.
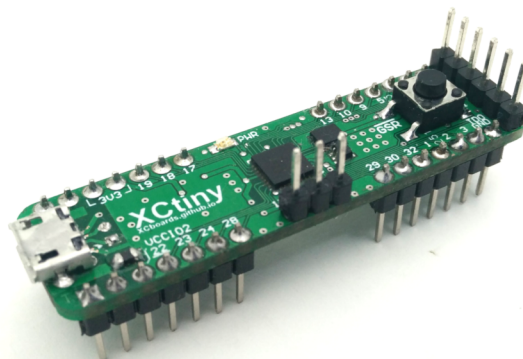

Figure 1: Assembled *XCtiny* board

2 DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
External supply voltage	V_{IN}	4.0	5.0	6.2	V
Supply current	I_{IN}		20	200	mA
I/O input voltage	V_I	-0.3		3.9	V
I/O source current	I_O			30	mA

3 AC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
On-board oscillator 0 clock frequency	f_{CLK0}		8.0		MHz
On-board oscillator 1 clock frequency	f_{CLK1}		7.8125		kHz

4 Board layout and components
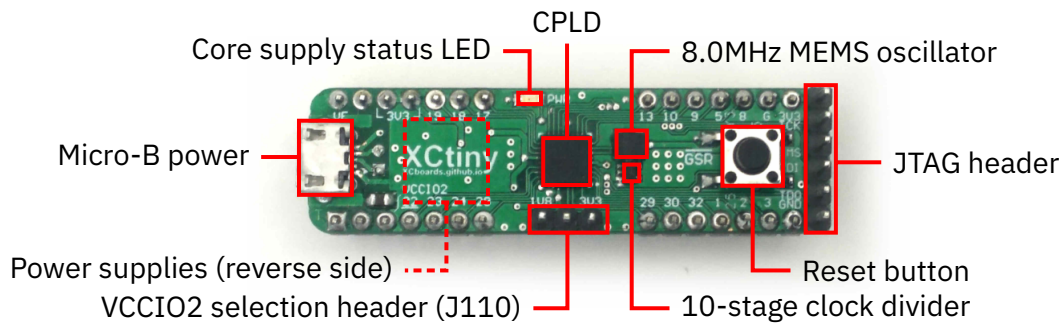
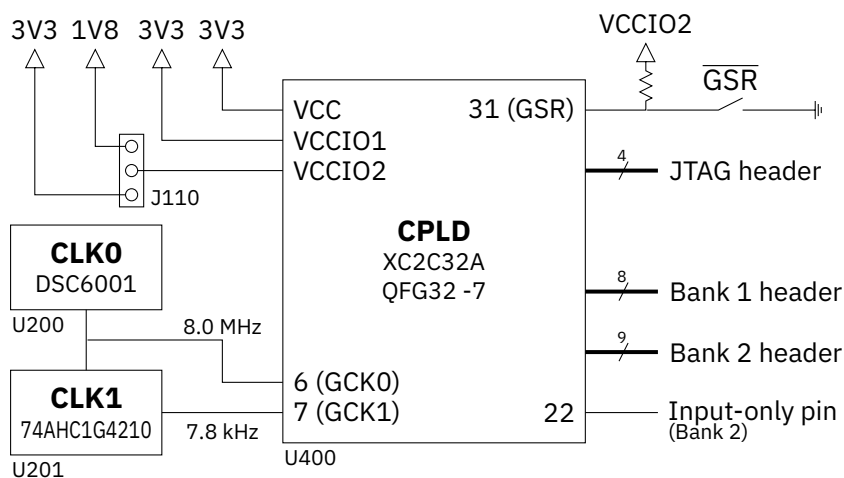Figure 2: *XCtiny* board (top view) component layout

Figure 3: Connection diagram of on-board peripherals

Visit **https://XCboards.github.io/XCtiny** for more information and further development resources.

Legal notice

This development board is intended for evaluation and development purposes in an electronics laboratory environment **only**. It does not constitute a finished product on its own, and hence may not comply with regulations applicable to finished products, including, but not limited to, directives regarding electromagnetic compatibility. The board is supplied "AS IS" without any warranties, with all faults, at the user's sole risk. The user assumes full responsibility and liability for proper and safe handling of the device. It is the user's responsibility to take any and all precautions regarding electrostatic discharge and any other technical or legal concerns.

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